HEWLETT PACKARD

MEMBER IrDA

Infrared Data Association

IrDAâ Control Compliant Peripheral Engine (PE)

PRELIMINARY

File: hsdl-7500_datasheet_v0.1au.pdf Thu Oct 1 15:57:41 SST 1998

Technical Data

HSDL-7500

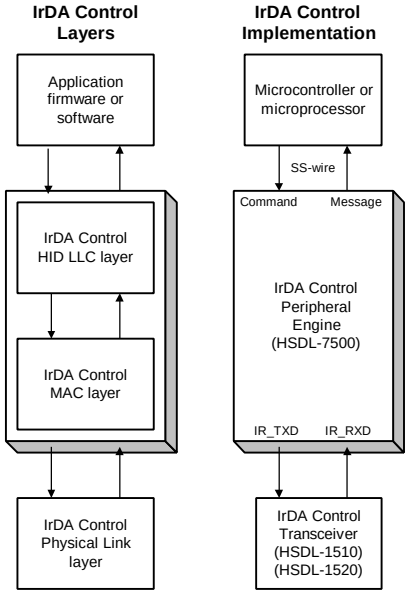
Features

- **Easy to use, all-in-one embedded communication controller**
- **Implements Endec, IrDA Control MAC layer, HID LLC layer**
- **All IrDA Control protocols available to a microprocessor or microcontroller via a simple command set.**
- **Simple 6-wire serial interface (SS-wire: Synchronous Serial wire) to mP/mC.**
- **Optimised interface to HP IrDA Control transceivers (HSDL-1510 and HSDL-1520).**
- **Low current consumption. I_{CC}=3mA during operation.**
- **Low supply voltage. V_{DD}=2.7 to 3.3V**

Applications

- **Enables wireless capability for computer peripherals**
- **Computer peripherals: Mice, keyboards, joysticks, trackpads.**
- **Home appliances & consumer electronics: Televisions, HiFi sets, microwave ovens, universal remote controls**
- **Optimised for HP IrDA Control transceivers (HSDL-1510 or HSDL-1520) to peripheral or host processor.**

Space reserved for HSDL-7500 photograph



Description

The HSDL-7500 provides an optimised one-chip interface between a µP/µC and an IrDA Control transceiver (HSDL-1510 or HSDL-1520). It supports the full IrDA Control MAC and HID LLC layer services in hardware, making it easy to implement the IrDA Control protocol (compliant with Revision 1.0e). The HSDL-7500 also performs the modulation and demodulation functions used to encode and decode the electrical pulses from the IrDA Control transceiver.

The PE can also be used in a host system, where it interfaces to a host µP/µC eg dongle to a host PC. Communication to the peripheral/host µP/µC is via a 6-wire serial interface with "Command" and "Message" attributes.

"Commands" are sent from the µP/µC to the PE, while the PE sends "messages" to the µP/µC. The message contents are the decode optical signals from the transceiver. Fig. 1 gives an overview of the connections and the grouping of I/O pins.

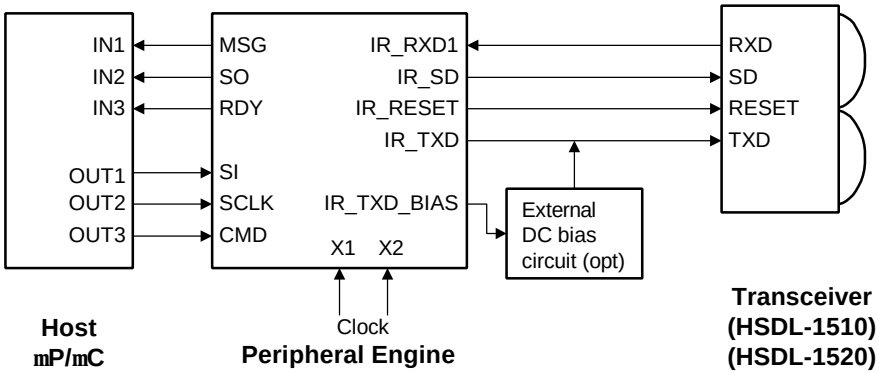


Fig 1: PE logical connection

Pinout

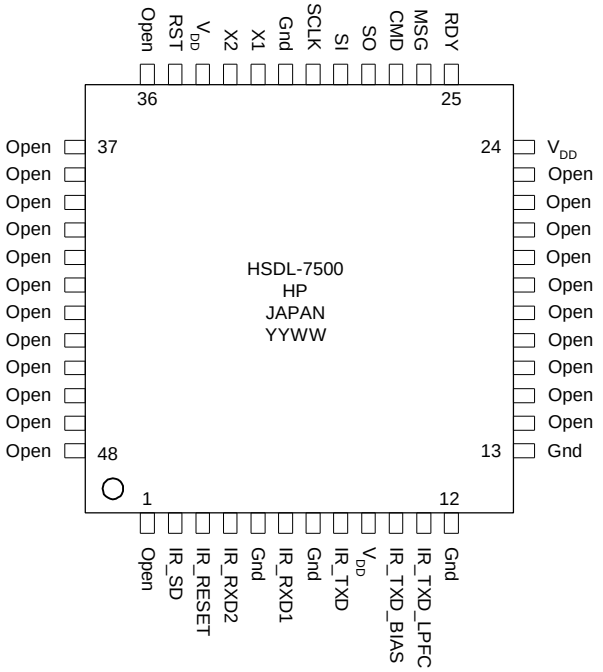


Fig. 2: HSDL-7500 Pinout

Functional Block Diagram

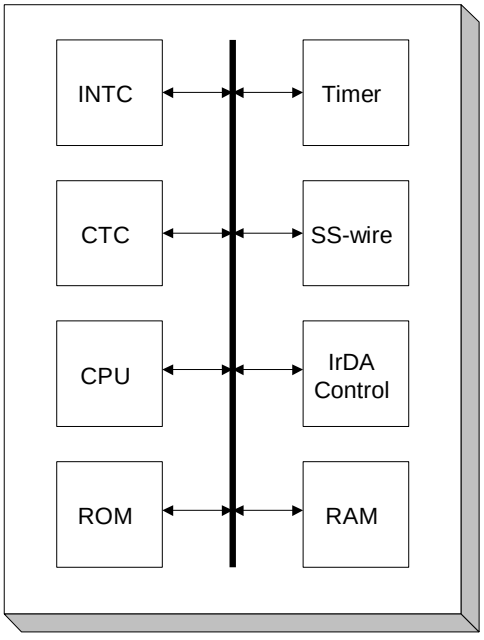


Fig. 3: HSDL-7500 Functional Block Diagram

I/O Pinout List

Pin	Name	Type	Function/Description	Notes
29	SI	In (SS-wire)	Serial input – from µP/µC	
28	SO	Out (SS-wire)	Serial output – to µP/µC	
30	SCLK	In (SS-wire)	Serial data clock, from µP/µC. Used to synch data transfers. When stopped SCLK=high.	
26	MSG	Out (SS-wire)	Signal to µP/µC that PE holds a message. Active high signal, condition as follows: • **PE holds msg**: PE asserts MSG. µP/µC must then issue Get_Message command to read in data. • **PE no msg:** PE de-asserts MSG.	
25	RDY	Out (SS-wire)	Signal to µP/µC for dataflow control. Active high signal, asserted when the next byte can be read/written through the data lines. The µP/µC must monitor the RDY line when it completes the last bit of the current byte. If RDY is not asserted the µP/µC should stop SCLK (SCLK=high) and wait until RDY is asserted.	
27	CMD	In (SS-wire)	Signal from µP/µC to indicate a command ID, active high. The µP/µC must assert CMD before sending bit D7 of the command ID to SI. After sending bit D0 of the command ID, the µP/µC must wait for RDY to be asserted, then de-assert CMD (low).	
8	IR_TXD	Out	Data to HSDL-1510/HSDL-1520 transceiver input (T_{XD} pin)	
10	IR_TXD_BIAS	Out	DC bias output for transceiver LED drive. (Use of DC Bias is not yet ratified in IrDA Control specification)	
11	IR_TXD_LPFC	Out	n/c	
6	IR_RXD1	In	Data from HSDL-1510/HSDL-1520 transceiver output (R_{XD} pin)	
4	IR_RXD2	In	n/c	
2	IR_SD	Out	Signal to shutdown HSDL-1510/HSDL-1520 transceiver (SD pin).	
3	IR_RESET	Out	Signal to reset HSDL-1510/HSDL-1520 transceiver receiver sensitivity (RESET pin).	
35	RST	In	PE hardware reset	
31	X1	In	Clock input (6MHz)	
33	X2	Out	n/c	
	V_{DD}		Power	
	Gnd		Chip ground	